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VOLTAGE SAG CHARACTERIZATION BY DWT BASED HDL MODEL

P. RAM KISHORE KUMAR REDDY

Associate Professor, Department of EEE, Mahatma Gandhi Institute of Technology, Hyderabad, Andhra Pradesh, India

ABSTRACT

Power quality is important for consistency and steadiness of power system. The effects due to switching transient are investigated in this paper. The DWT based techniques are recommended to analyze the transient effects and to improve the quality of power system and its protection. These measures were efficient in providing better solution at the cost of high resource consumption. High resource consumption results in slower response while analyzing power system. A FPGA based DWT architecture is recommended to improve the performance of response in the power system. The Field Programmable Gate Arrays (FPGA) based DWT architecture is proposed with theoretical results from MATLB and was observed to be meeting the accuracy of estimation.

KEYWORDS: Power Quality, Voltage Sag, Wavelet Transform, Digital Modeling, VHDL

INTRODUCTION

The electric power requirement is increasing due to increase in demand from electrical utilities. In recent years power quality is one of the primary concerns of the utilities, since lack of quality in power may cause malfunctions, instability, short lifetime, and so on. In past ten years it is observed that the most important causes which take the responsibility for the power system failures are disturbances[1] in power systems. In order to get better electric power quality, the sources and causes of faults must be known for corrective measures. The first step is to detect and localize various power quality disturbances. In order to resolve a possible solution the disorder must be monitored, captured and classified properly. Feature extraction of the signal is very vital and can be done by transforming the raw signals with appropriate mathematical method.

Due to sudden disturbances voltage sag is developed and is characterized by its magnitude and duration. A Common cause of sag include starting of large induction motors, transient faults which leads to increase in the magnitude of and current consequently pose the problem of voltage drop[4]. Exact and fast voltage sag recognition is an essential behavior of voltage compensator in determining the beginning and ending of voltage sag event. Many methods such as Hysteresis voltage control, RMS value evaluation technique, Missing Voltage technique, Peak evaluation technique have been proposed in literature for the detection of voltage sag in terms of magnitude and frequency. Hysteresis voltage control poses a problem of dead band which can be avoided by RMS value evaluation technique due to its post-event window technique.

All of the conventional methods may give appropriate analysis of voltage sag but for automation of the analysis, they may require refinement[5]. Due to this it is appropriate to approach for signal processing tools which are not only identify abnormality but also will provide flexibility for computerization.

The sampled voltage or current waveforms offer quantitative descriptions of power quality in terms of the foremost harmonic components and their associated magnitudes. The quantitative description will give information regarding the points where disturbances begin and end. For this, signal processing tools based on transform or sub-band

filter method and model based methods can be used[2]. In general signal processing tools are convenient for quantitative descriptions of power quality problems.

WAVELET TRANSFORMATION

In order to detect and analyse the power quality problems such as voltage sags. The fundamental idea of using wavelets is to analyze the signal at different scales or resolutions called Multi Resolution Analysis. Wavelets are a class of functions used to localize a given signal in both space and scaling domains. Compared to windowed Fourier analysis, the basis wavelet is stretched or compressed to change the size of the window. Thus wavelets automatically adapt to both the high frequency and the low-frequency components of a signal by different sizes of windows.

Any small change in the wavelet representation produces a correspondingly small change in the original signal, which means local disturbances do not influence the entire transform. The wavelet transform is suitable for analyzing non-stationary signals such as voltage sag, swell, transients, flicker etc. Wavelets are functions generated by dilations and translations of a single function ψ called a mother wavelet,

$$\psi_{a,b}(x) = \frac{1}{\sqrt{a}}\psi(\frac{x-b}{a})$$

The basic idea of wavelet transform is to signify any arbitrary function 'f' as a decomposition of the wavelet basis or write 'f' as an integral over a and b of $\psi_{a,b.}$ Wavelet Transform (WT) is applied to analyze non-stationary signals, i.e., whose frequency response varies in time.

Although the time and frequency resolution problems are results of a physical event and exist despite of the transform used, it is possible to analyze any signal by using an alternative approach called the multi resolution analysis (MRA). MRA analyzes the signal at different frequencies with different resolutions. MRA are basically designed to give good time resolution and poor frequency resolution at high frequencies and good frequency resolution and poor time resolution at low frequencies .This approach is useful for especially voltage sag if the signal considered has high frequency components for short durations and low frequency components for long durations[8].

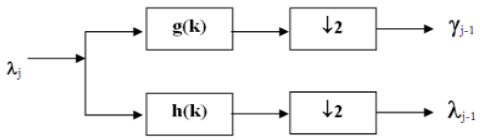

Figure 1: Realization of One Stage Iterated Filter Bank

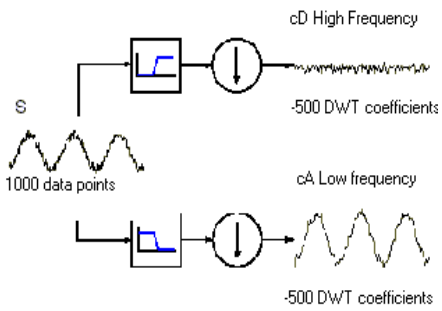

Figure 2: Decomposition of Signal with Noise Showing cD and cA

One way to built sub-band codification is to split the spectrum into frequency bands. But it is convenient to split the given signal into two bands of spectral components such as low pass filtered and high pass filtered components.

The high pass filtered components gives the smallest information where as low pass filtered components gives information regarding further minutely varying details until desired number of bands.

In the above scheme the disadvantage is that the signal spectrum coverage is fixed .To avoid this decomposition of the signal is used which is illustrated ain Figure 2. For a sample current signal with a noise parameter the decomposition is shown in figure 2. The detail coefficients cD are consisting high-frequency content and the approximation coefficients cA contain the low frequency content of the signal. The actual lengths of the detail and approximation coefficients are slightly more than half the length of the original signal. Thus the filtering process is implemented by convolving the signal with a filter. By observing the features obtained by Discrete Wavelet Transform (DWT) it is easy to detect, locate and classify the power quality disturbances This MRA can be performed by Discrete Wavelet Transform (DWT).

IDENTIFICATION OF VOLTAGE SAG

Different voltage sags have been created in MATLAB environment. Using DWT ‘db4’ at level 5 Signals have been processed for characteristics of voltage sag. Figure 3 represents the approximate and detailed coefficients of healthy signal and Figures 4 represent the approximate and detailed coefficients of the signal with a dip of 10%.

In addition to approximate coefficients, detailed coefficients also evaluated for high resolution analysis of the signal. Filter Bank architectures are realized to perform MRA in real time application using filter chips (or) DSP processors[9]. Both the approaches provide resolution information but high power consuming and slower in response due to delay in data transfer. The delay in response delay may result in improper operation of electrical control device resulting in lowering of life-cycle for costly and reliable electrical equipments.

To reduce the above difficulties associated with the traditional DSP Processors or filter chips, Field Programmable Gate Arrays (FPGA), which offers the potential of designing high performance system at low cost.

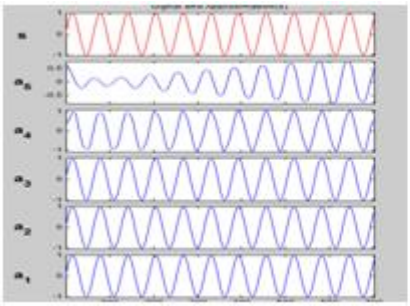

Figure 3: Approximate Coefficients of Healthy Signal

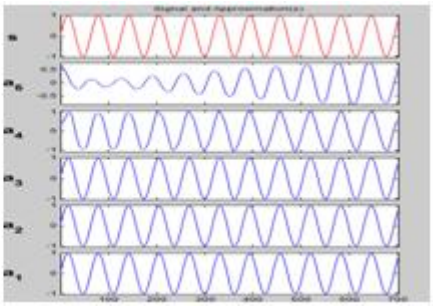

Figure 4: Approximate Coefficients of Signal with 10% Sag

DIGITAL MODELING OF DWT

For the realization of the stated DWT architecture, the filter bank architecture is developed using VHDL coding. The discretized current pulse is passed as input to this system in 16 bit floating represented in excess-7 notation. The samples are buffered into the input FIFO of and are passed to the filter bank via buffer logic. The inputs are off-centered by two and are passed as a block of 4 samples per cycle. These samples are buffered into the buffer logic and are passed to the filter bank on request generation. A pair of High pass and a Low pass filter bank is realized for each level of decomposition.

Each wavelet coefficient is decomposed by a factor of 2 before passing it to the sample RAM. The sample RAM is developed with 12 x 16 location for holding the wavelet coefficient after every high pass filter output. The filter logics

are realized using MAC (multiply and accumulate) operation where a recursive addition, shifting and multiplication operation is performed to evaluate the output coefficients.

The filter logics are realized using MAC (multiply and accumulate) operation where a recursive addition, shifting and multiplication operation is performed to evaluate WT coefficients.

Before passing the data to filter bank the FIFO logic realized for storing the data in asynchronous mode of operation, operating on the control signals generated by the controller unit. On a read signal the off-cantered data is passed to the buffer logic.

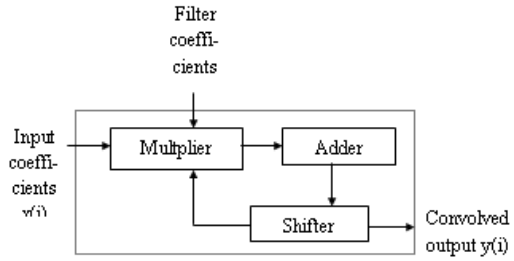

Figure 5: Realization of Recursive MAC Operation

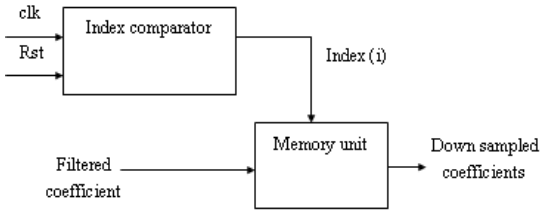

Figure 6: Architecture for Decimation by 2 Logic

The obtained detail coefficients are down sampled by a factor of two to reduce the number of computation in turn resulting in faster operation. To realize the decimator operation comparator logic with a feedback memory element is designed as shown in Figure 6.

VHDL MODELING TO REALIZE DWT

The proposed system is realized using VHDL language for it's functional definition. The HDL modeling is carried out in top-down approach with user defined package support for floating point operation and structural modeling for recursive implementation of the filter bank logic. For the realization a package is defined with user defined record data type as

typereal single is

record

sign : std_logic;

exp: std_logic_vector(3 downto 0);

mantissa: std_logic_vector(10 downto 0);

end record;

The floating-point addition, multiplication and shifting operation are implemented as procedures in the user defined package and are repeatedly called in the implementation for recursive operation

procedure shifftl (arg1: std_logic_vector;arg2: integer;arg3 :out std_logic_vector);

procedure shifftr (a:in std_logic_vector; b:in integer;result: out std_logic_vector);

procedure addfp (op1,op2: in real_single;op3: out real_single) ;

procedure fpmult (op1,op2: in real_single;op3: out real_single) ;

For performing the convolution operation, filter coefficients are defined as constant in this package and are called by name in filter implementation. For the evaluation of the implemented design the test vectors are passed through the test bench generated from Matlab tool.

The continuous output of secondary side transformer obtained after impulse test are discretized using Matlab tool where each coefficient is converted to 16-bit floating notation and passed to the test bench for HDL interface. The coefficients obtained from the filter bank after convolution is then compared with the results obtained from the MATLAB decomposition for accuracy evaluation.

RESULTS

The sampled input data (Voltage Sag) and the comparison of subsequent wavelet coefficients from MATLAB Program, HDL code is as shown below:

Table 1: Input Data

Output from Impulse Test as Input	Digital Binary Data
0.01751	‘0’,”1010”,”11000000001”
0.0158	‘0’,”0110”,”00001100001”
0.0365	‘0’,”0101”,”01100101000”
0.1325	‘0’,”0100”,”01001110001”
0.1245	‘0’,”0110”,”01001100000”

Table 2: Detail Coefficients at Level 1

Matlab Coeff.	HDL Output (Binary)	Decimal Equivalent
0.15122	‘0’,”1001”,”00111100110”	0.15171
0.003154	‘0’,”0100”,”00010111101”	0.003111
0.1233	‘0’,”1001”,”01101010110”	0.1243
0.2259	‘0’,”0111”,”00010100010”	0.2214
0.003114	‘0’,”1000”,”00011010001”	0.003112

Table 3: Detail Coefficients at Level 2

Matlab Coeff.	HDL Output (Binary)	Decimal Equivalent
0.2110	‘0’,”1010”,”01010111000”	0.2101
0.00114	‘0’,”0011”,”00001001001”	0.00121
1.0023	‘0’,”0100”,”00010111000”	1.0014
-0.035	‘1’,”0110”,”00101100000”	-0.034
-0.02143	‘1’,”0100”,”00011111001”	-0.02143

Table 4: Detail Coefficients at Level 3

Matlab Coeff.	HDL Output (Binary)	Decimal Equivalent
0.2243	‘0’,”1000”,”00011000110”	0.22
-0.601	‘1’,”0011”,”01000011101”	-0.6092
-0.0024	‘1’,”0111”,”00010001000”	-0.0023
0.104	‘0’,”0101”,”00011000001”	0.110
0.0323	‘0’,”0100”,”01000001000”	0.0324

Table 5: Approximate Coefficients

Matlab Coeff.	HDL Output (Binary)	Decimal Equivalent
0.224	'0','0100','01000010001"	0.2243
-0.0874	'1','1001','00000111000"	-0.0876
-0.02144	'1','0101','01000100000"	-0.0212
0.224	'0','0011','10000010001"	0.225
0.4557	'0','0110','00010011100"	0.4543

From the above table it can be observed that the WT coefficients using MATLAB and HDL are almost equal. Thus WT techniques are suited to analyze power quality problems and the logic can be realized by using filter bank architecture.

CONCLUSIONS

The power quality problem such as voltage sag is created by modeling power system network using MATLAB. Voltage sag characterization is expressed by change in magnitude, frequency and the duration. The hidden information from the voltage sag signal can be best extracted by using DWT by MATLAB and obtained WT coefficients. In order to atomize the voltage sag analysis, the DWT based digital model is realized. The proposed digital model is simulated in HDL environment and it is observed that WT coefficients of voltage sag signal using MATLAB is same as that of the HDL simulations.

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